Energy Efficient Smart Wireless Sensors Network

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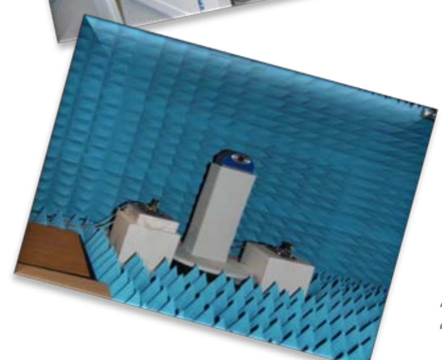
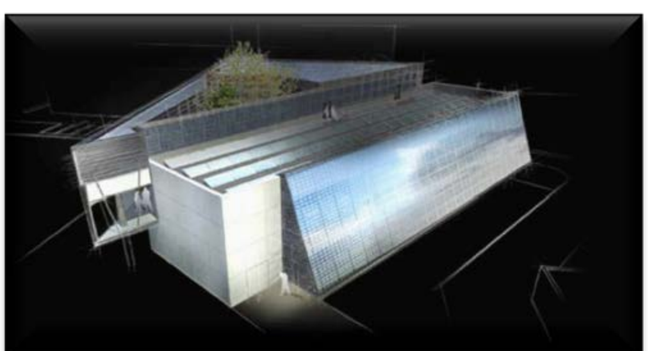
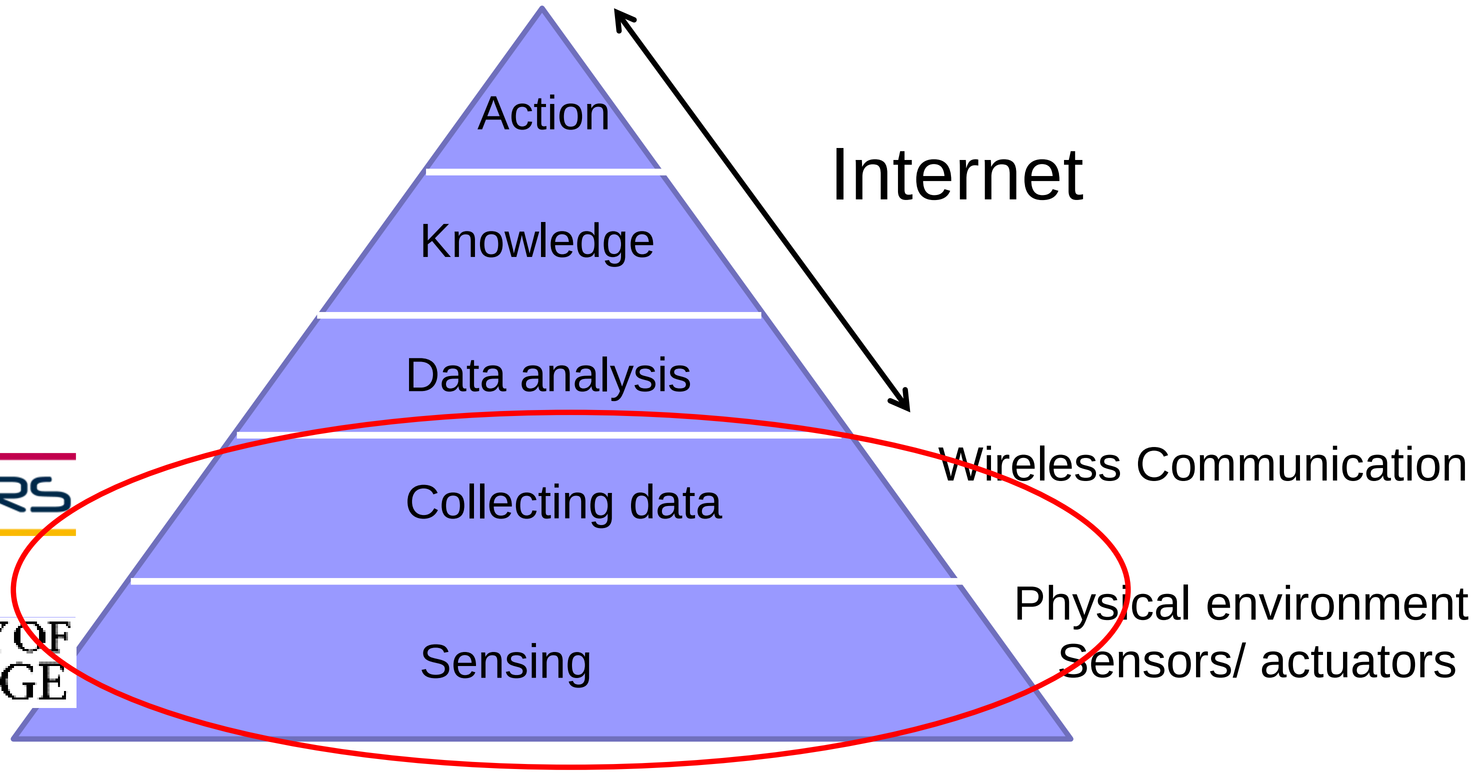
LAAS-CNRS laboratory

- 600 persons, 220 researchers
- Carnot institute - excellent relationship with the industry
- 1500 m^2 clean room
- Characterization center
- ADREAM platform for cyber-physical systems (from sensors to robots), autonomous in energy





IoT architecture



LAAS-CNRS

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<u>Our project objective</u> : develop a new platform to accommodate innovative CMOS sensors together with wireless systems to obtain energy efficient, reconfigurable WSN for many real-world applications

Challenges – research fields

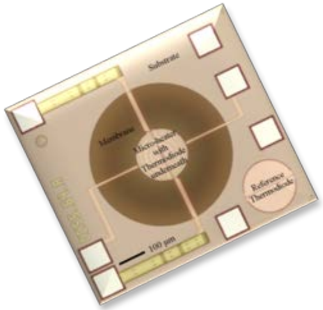
Real world, high scale deployment

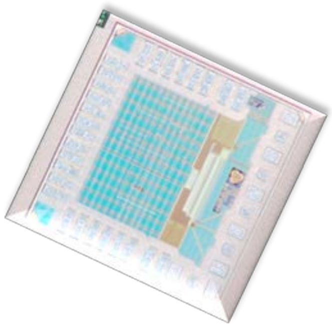
Energy efficiency

Toward Zero Power = ultra low power consumption + energy harvesting

Low power sensors

Energy efficient wireless communication architectures

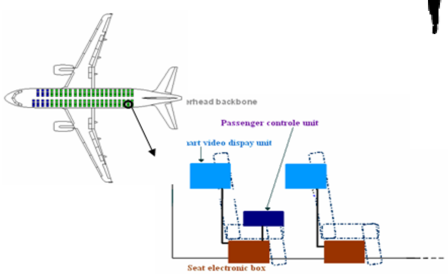


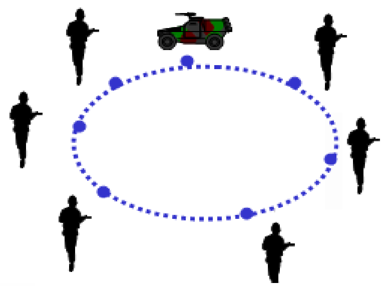


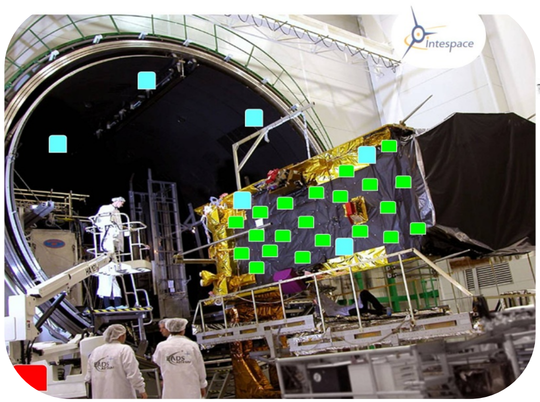
CMOS Integration (low cost, large area electronics)

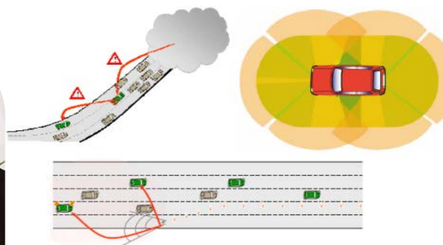
Small size and flexible integration

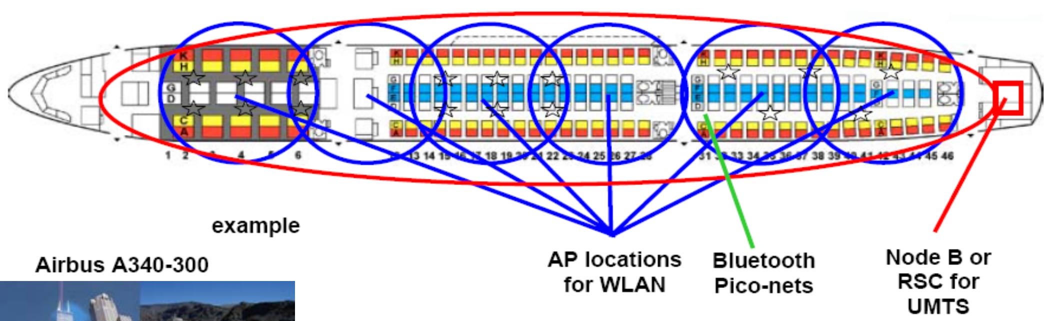
Numerous industrial applications











example

Airbus A340-300

Proposed design approach

- **Major driver : energy efficiency**
  - IR-UWB communications using nano-metric CMOS technology

- Application specific hardware → reconfigurability (MAC and physical layer)

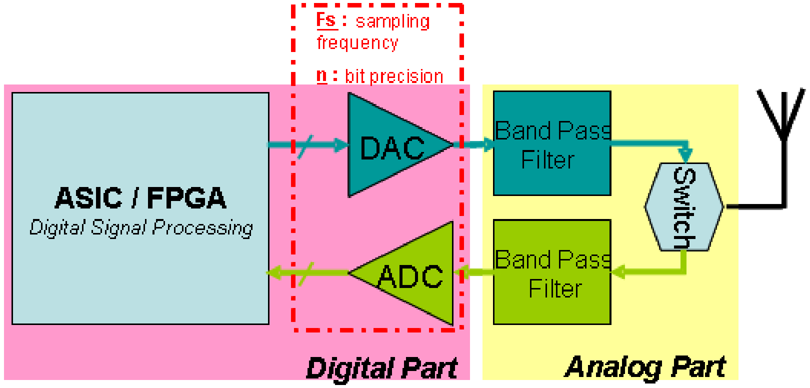
- Include new Services such as:
  - **Localization**
  - **Synchronization, time stamp**
  - **Safety, security**

- System approach: Cross-layering between low network levels (PHY and MAC) and high network levels (routing)

Ultra Wide Band Impulse Radio Transmission for WSN

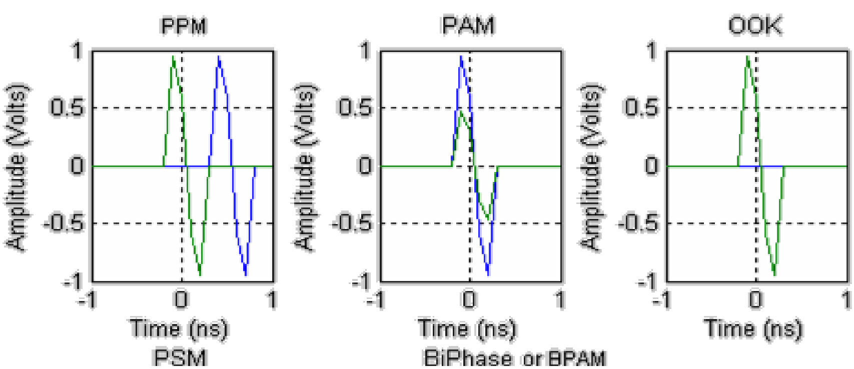
The advantages of IR-UWB

- Low level discontinue transmission
  - Low power transmission
  - Large frequency band
  - Very short pulse
  - Lower interference probability
  - Fine temporary resolution
    - Localization



Mostly Digital Radio Architecture

- Low complexity circuits to be developed in CMOS technology → low cost, low power
- Challenges :
  - Channel estimation
  - Fast DAC/ADC
  - Reception synchronization



Patent

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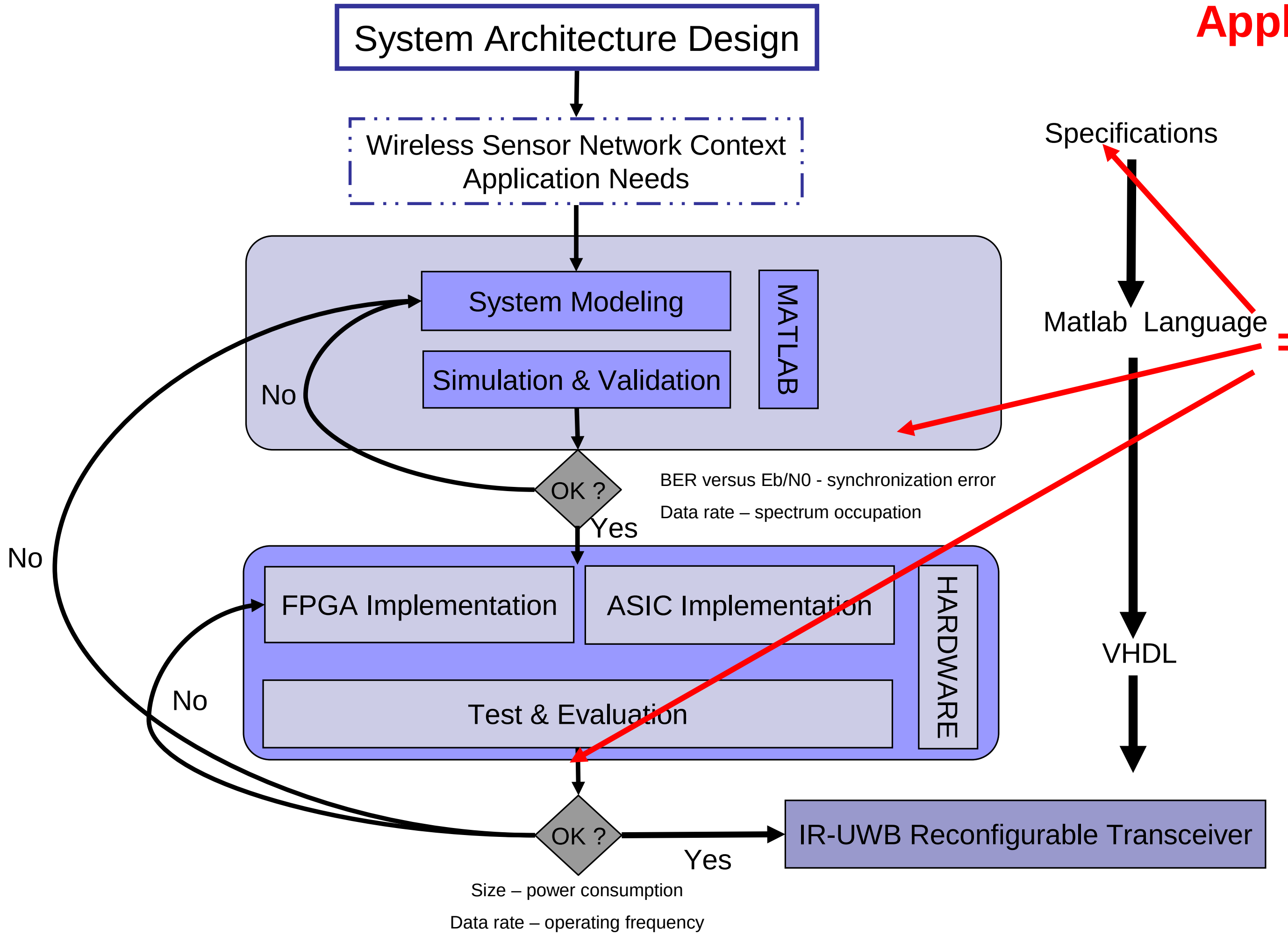
From system to hardware



Applications requirements :

-Data rate

-E/R distance

- Frequencies used

-...

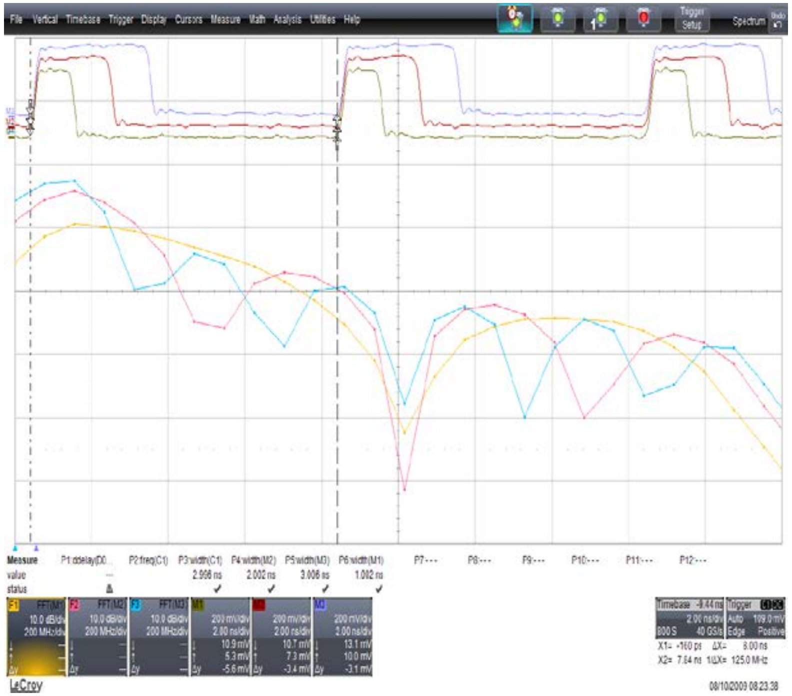
= +

Application	**Structure Health Monitoring**	Units
Regulation on mean EIRP	-41,30	dBm/MHz
Distance	50,00	m
Data rate	1,00	Mbits/s
Low frequency	3,10	GHz
High frequency	6,85	GHz
Center frequency	4,98	GHz
Bandwidth	3,75	GHz
Pulse duration	0,27	ns
Time slot duration	1000,00	ns
Duty cycke	0,0267	%
Mean EIRP	-5,56	dBm
Max. EIRP	30,18	dBm
Tx antenna Gain	3,00	dB
Rx antenna Gain	10,00	dB
Power max. feed to antenna	522,47	mW
Channel	Industrial LOS	
Channel path loss	86,11	dB
Boltzmann constant	1,38E-23	J/K
Temperature	213,50	K
Thermal Noise density	-175,31	dBm/MHz
Available Eb / N0	**69,38**	dB
Supported delay spread	**999,73**	ns

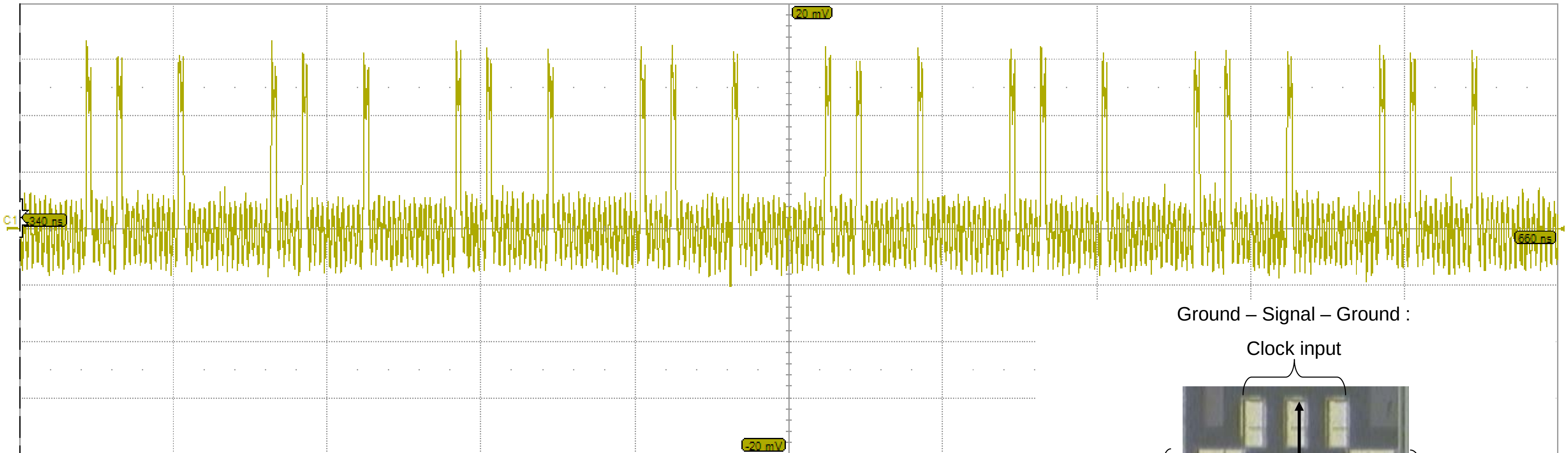
Link Budget

FPGA prototypes

- IR-UWB multi user emitter and receiver
- IR-UWB receiver with localization function
- IR-UWB reconfigurable transceiver in modulation, pulse duration, spectral occupation, data rate and user code
- IR-UWB reconfigurable transceiver at 120Mb/s – state of art: 50Mb/s (Electronics Letters, March 2010)



Measurements of first UWB IR emitter performances



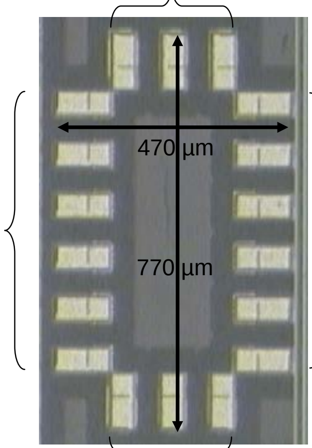
Measured results :

Data rate : 8 to 375 Mbits/s

Tp : 20 ns to 720 ps

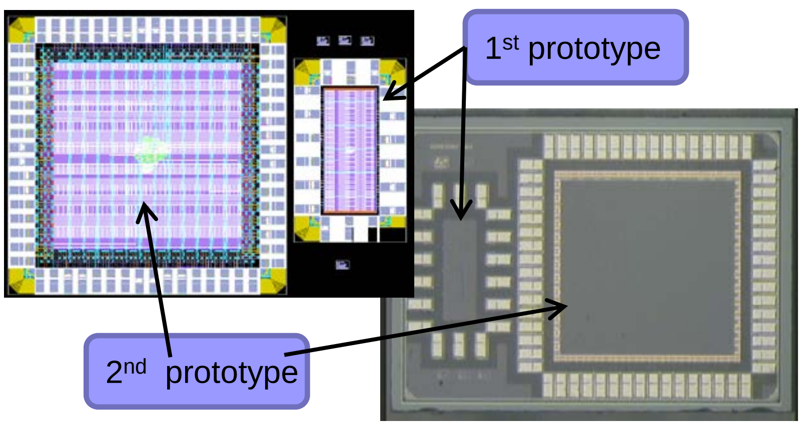
Consumption: 60 µW to 515µW

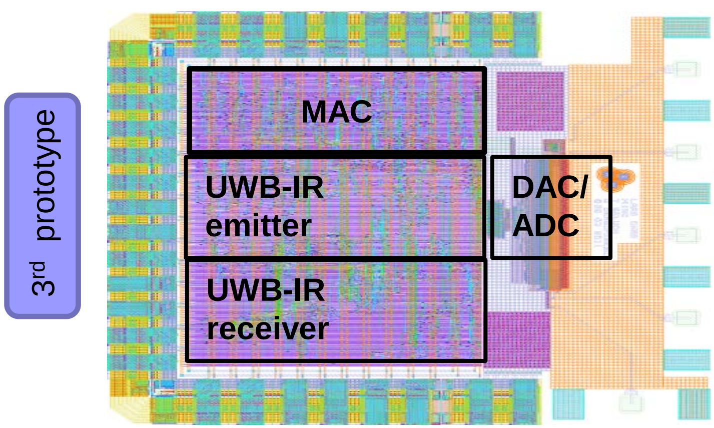
FOM: 7.23 to 1.4 pJ/bit



Low power ASICs - emitter/receiver IR-UWB

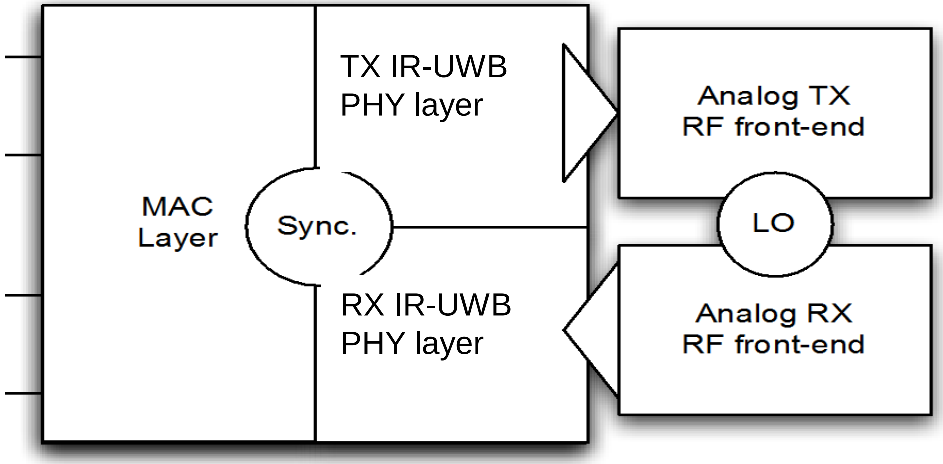
- UWB-IR emitter – CMOS 65 nm STMicro. technology .Low complexity digital design : fast and reliable
- 1^{st} emitter prototype : without DAC, 1 bit output, OOK modulation
- 2^{nd} emitter prototype: reconfigurability in data rate (up to 1 Gbps), modulation, impulse form, impulse duration.;
- **3^{rd} emitter /receiver prototype: with DAC/ADC and MAC layer**



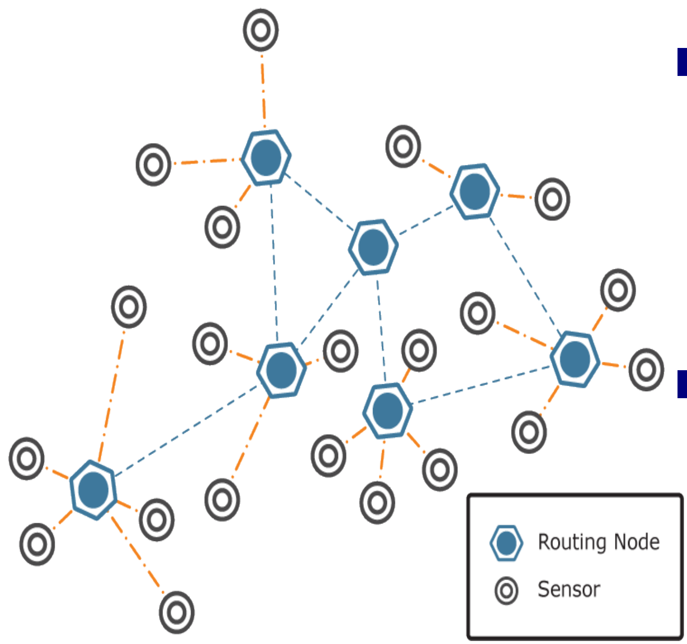


Simulated power consumption < 40 mW for a data rate up to 500Mbits/s

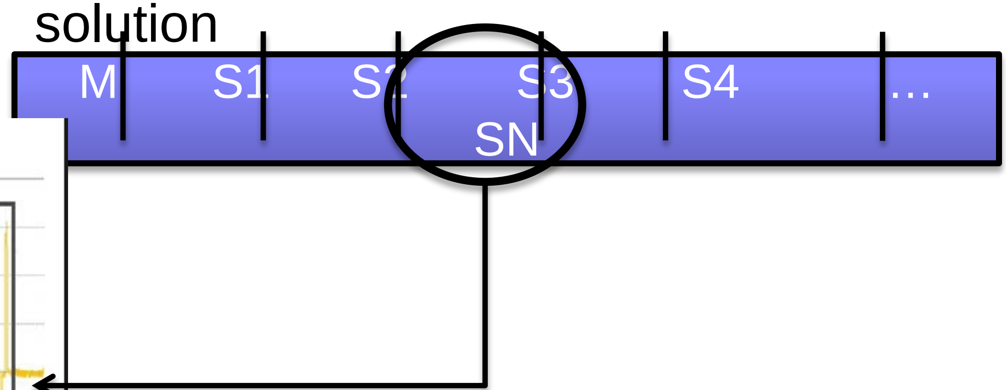
MAC layer and clock synchronisation for IR-UWB

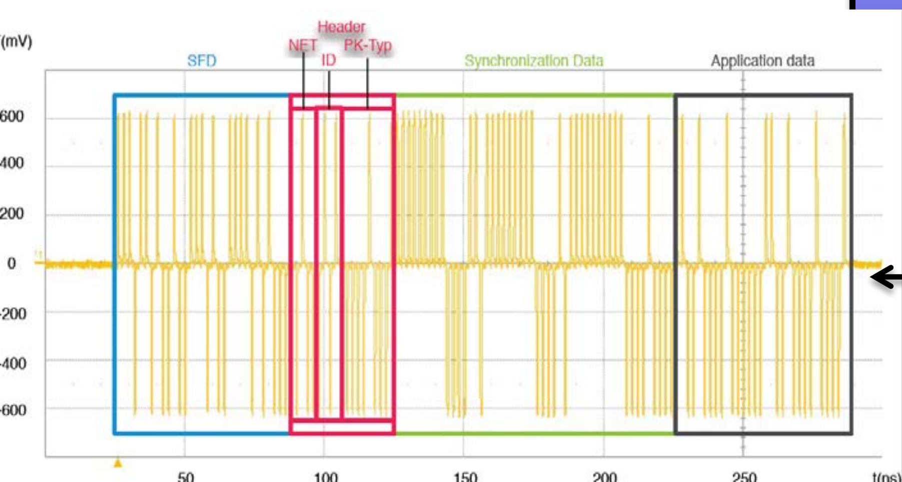


TDMA MAC layer
Clock synchronization for real time measurements

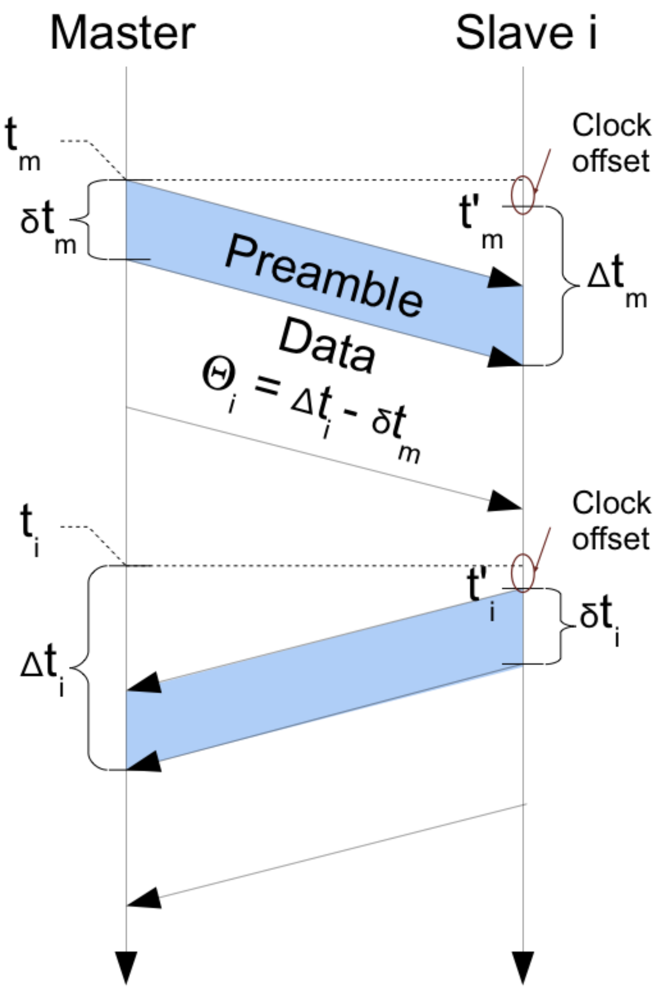


- Context:
  - Static cluster tree network
  - No mobile nodes
  - Clock synchronization needed
- Solution:
  - TDMA
  - WiDeCS Sync Protocol – LAAS-CNRS solution





Cross-layer design
WiDeCS synchronization



- Goals:
  - Compensate clock offset
  - Estimate transmission latency and compensate its variations
- Solution:
  - 2 way ranging
  - Periodic update
  - Timestamp 1st effective bit instead of 1st bit of preamble

$$\Delta t_{clk} = \frac{(\Delta t_i + \delta t_m) - (\delta t_i + \Delta t_m)}{2}$$

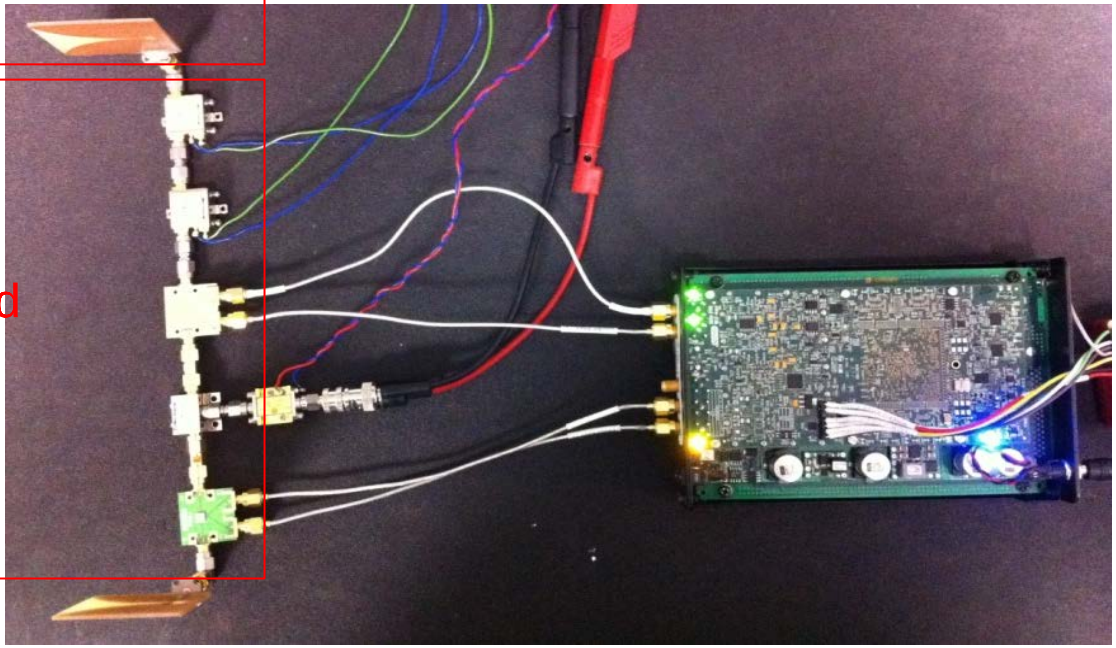
$$\Delta t_{clk} = \frac{\Theta_i - (\delta t_i + \Delta t_m)}{2}$$

FPGA prototype: TDMA Mac layer, IR-UWB transceiver, clock synchronization

❖ Wireless communicating node FPGA prototype

Antenna

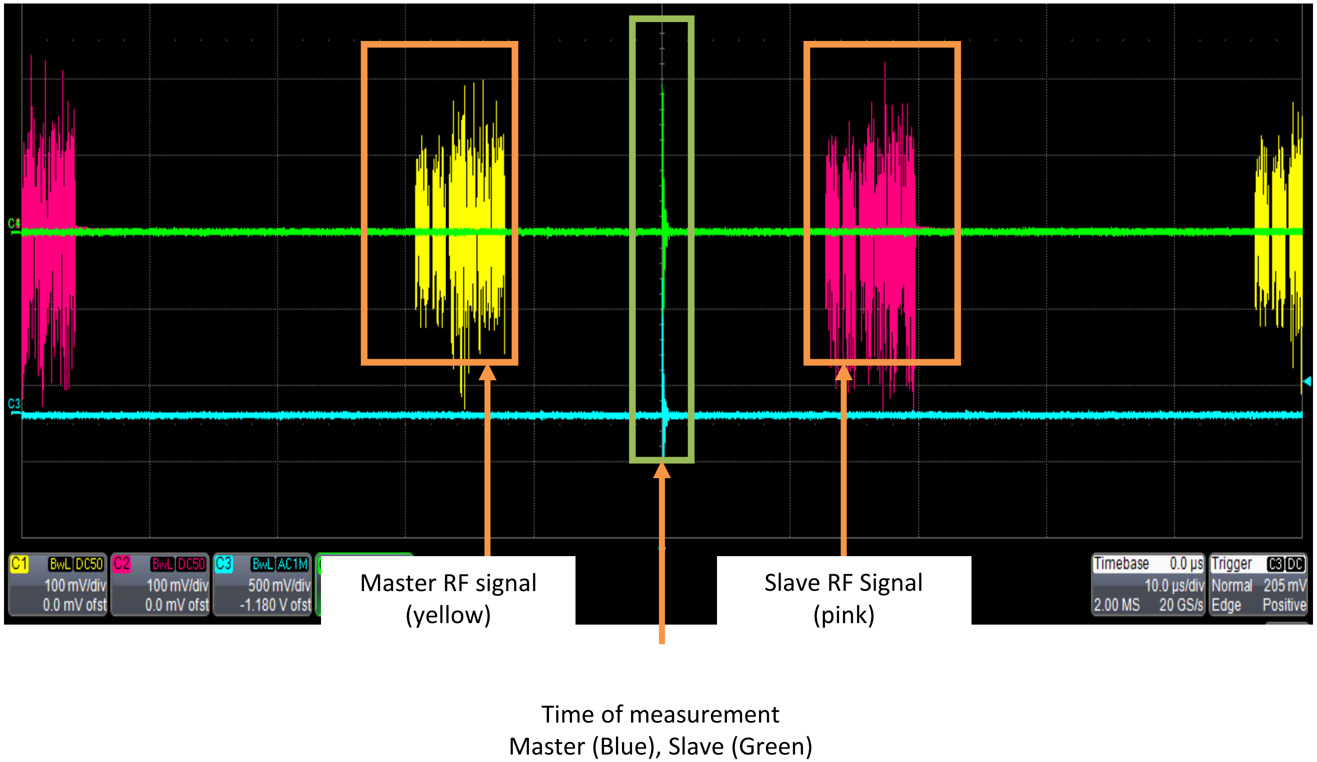
RF front end



- RedRapids boards with Virtex 4 and DAC/ADC
- IR-UWB
- TDMA MAC layer
- WiDeCs synchronization protocole

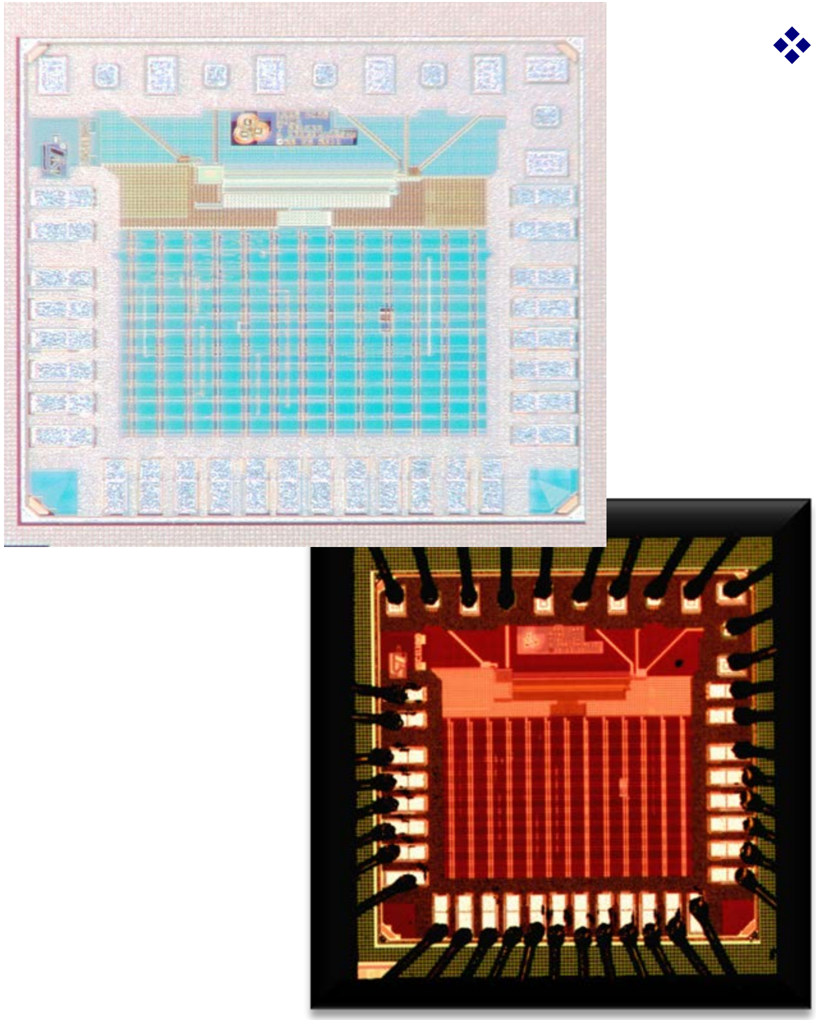
FPGA prototype with MAC layer and clock synchronization using UWB transmission

- Scope measurement prove clock synchronization → good accuracy in ToF measurements



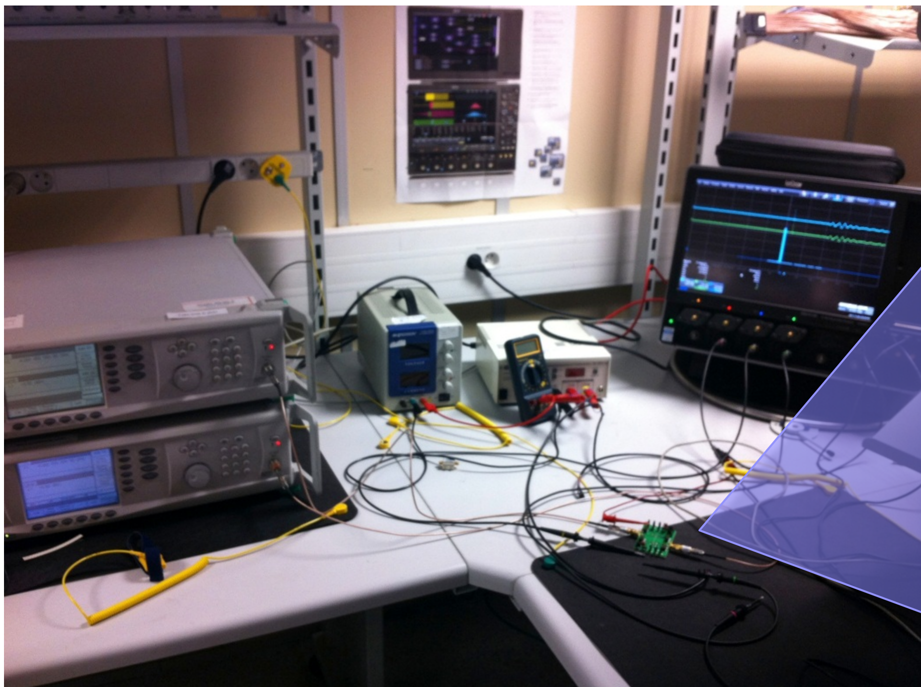
See demo for clock synchronization and for aircraft in flight test at http://www.laas.fr/~daniela → News (April 2012)

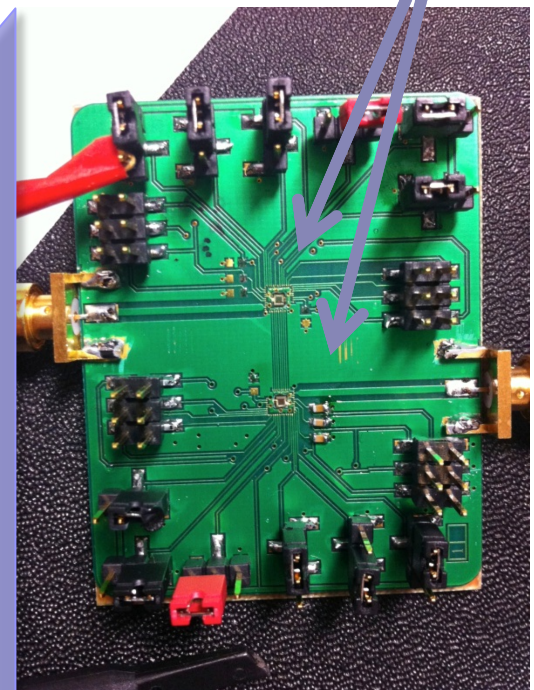
ASIC prototype: MAC layer, clock synchronization and IR-UWB transceiver



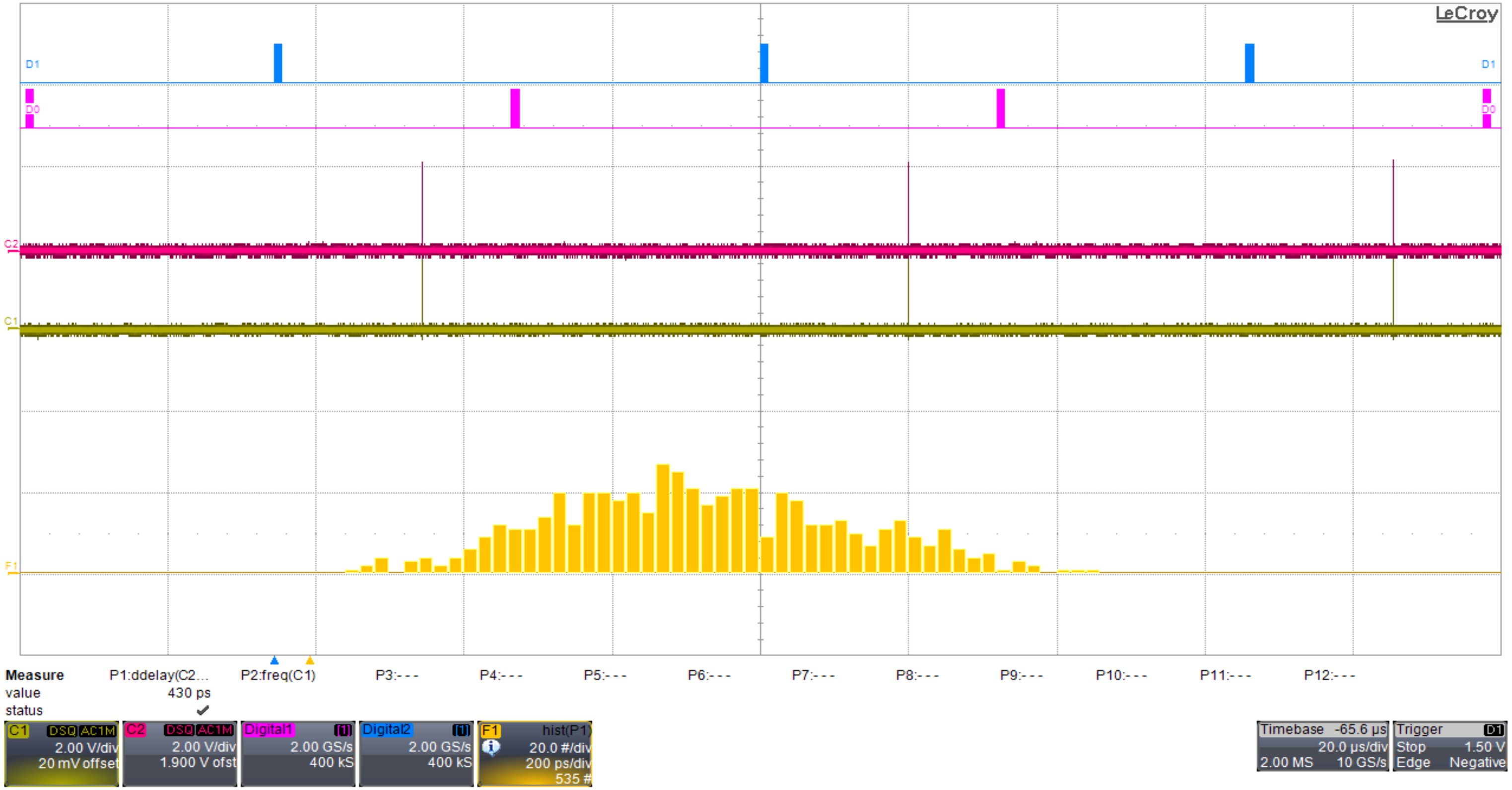
- 1 mm^2 chip with
  - PHY layer: IR-UWB BPSK transceiver
  - TDMA MAC layer
  - Clock synchronization
  - Fast ADC/DAC
  - Mixte SoC
  - Build to interface with RF front-end

Test platform





Measurements results



P_c = 50 mW

Max data rate: 500Mbps

Energy/bit: 100 pJ/bit (best case)

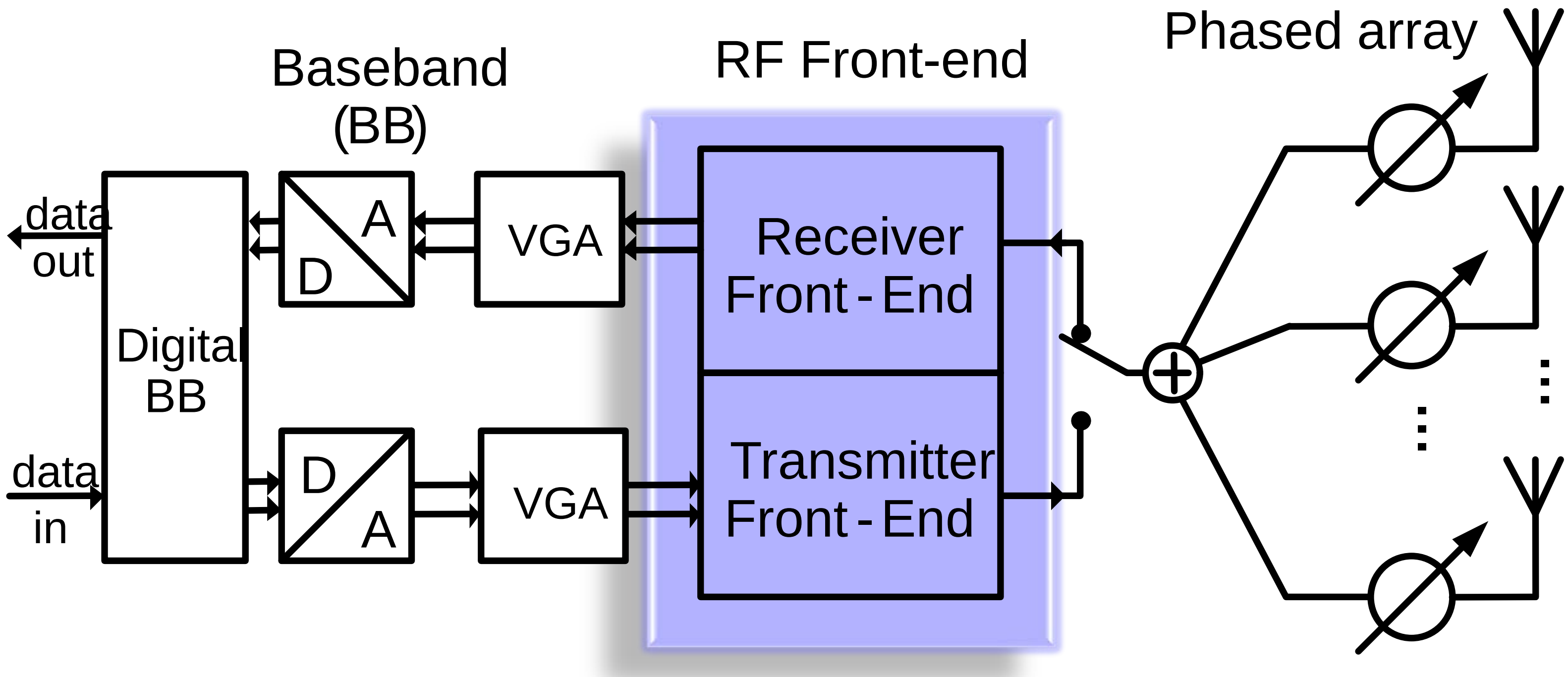
Clock synchronization precission ~ 1 ns

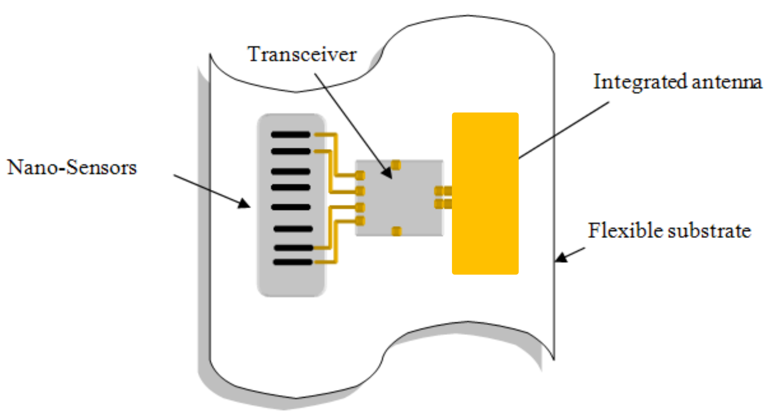
SoC IR-UWB @ 60GHz

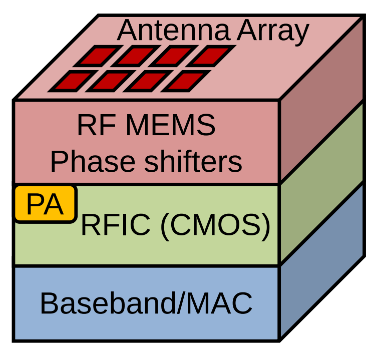
60GHz communications enabled by nano-metric CMOS technology

- Short transmission range and high directivity →Low interferences between nodes
- High number of communicating nodes in a small area
- CMOS 65 nm technology →Low power consumption, Low cost

SoC IR-UWB @ 60GHz



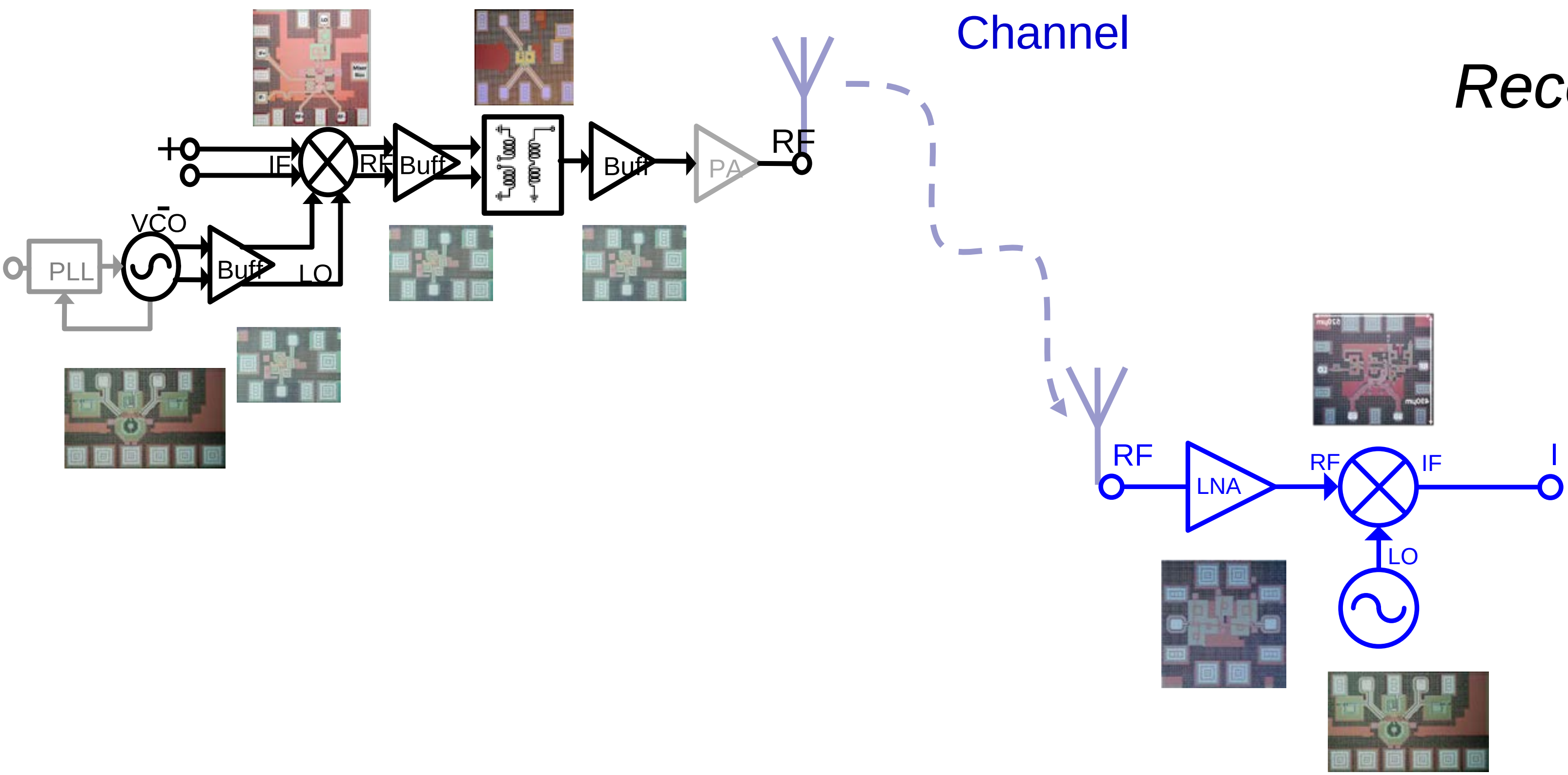




Architecture of 60GHz Front-end

Transmitter

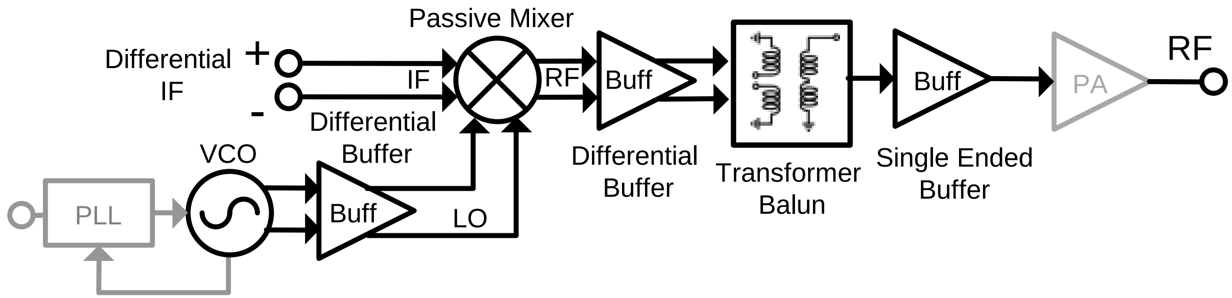
Receiver

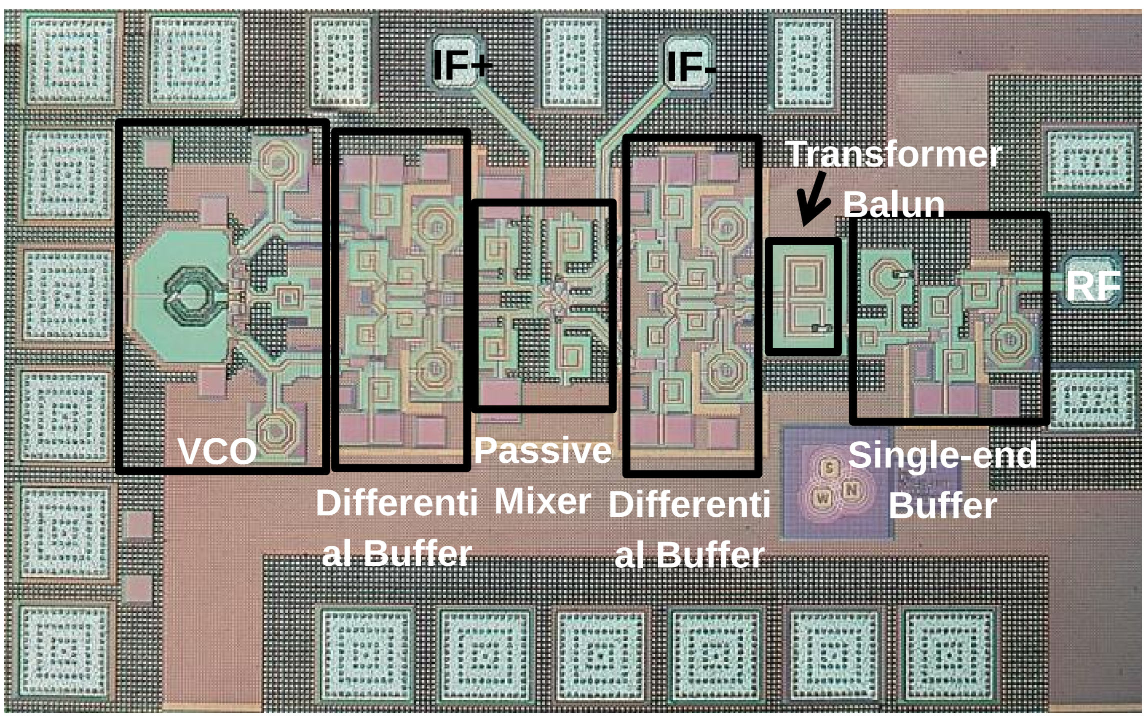


- Direct Conversion Topology
- Implementation in 65 nm CMOS

Small size
Low power consumption

Ultra low power 60GHz Transmitter





Performances of the chip:

- Bias Voltage = 1.2 V
- **Power consumption = 53 mW**
- Conversion gain > 5dB @60GHz
- Bandwidth ~10 GHz
- Size: 0.6 mm^2

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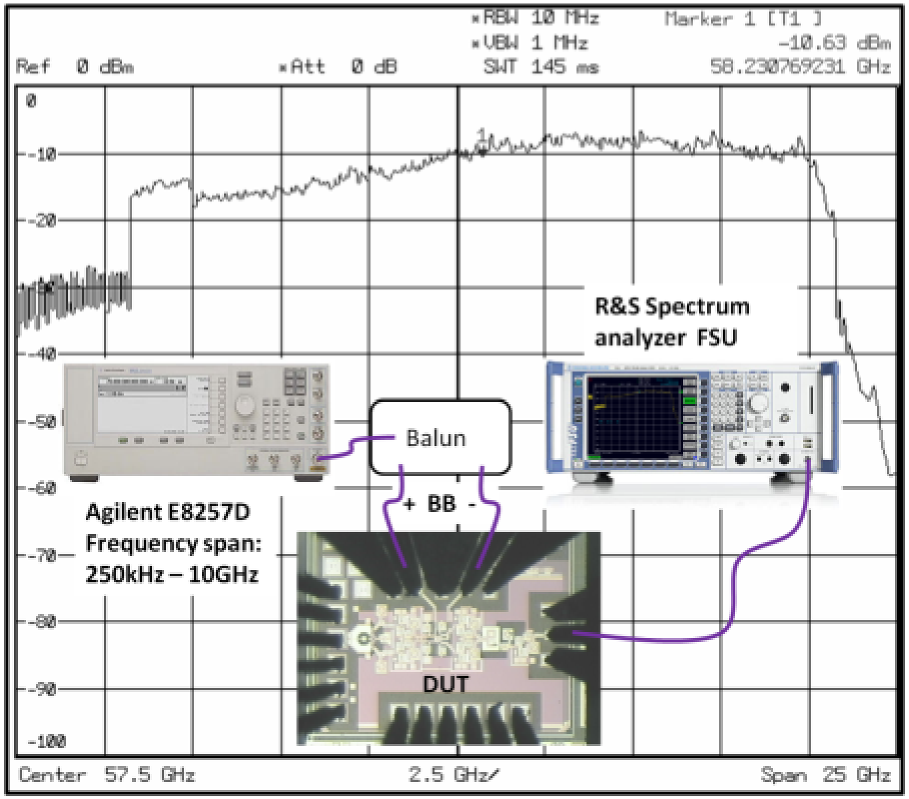
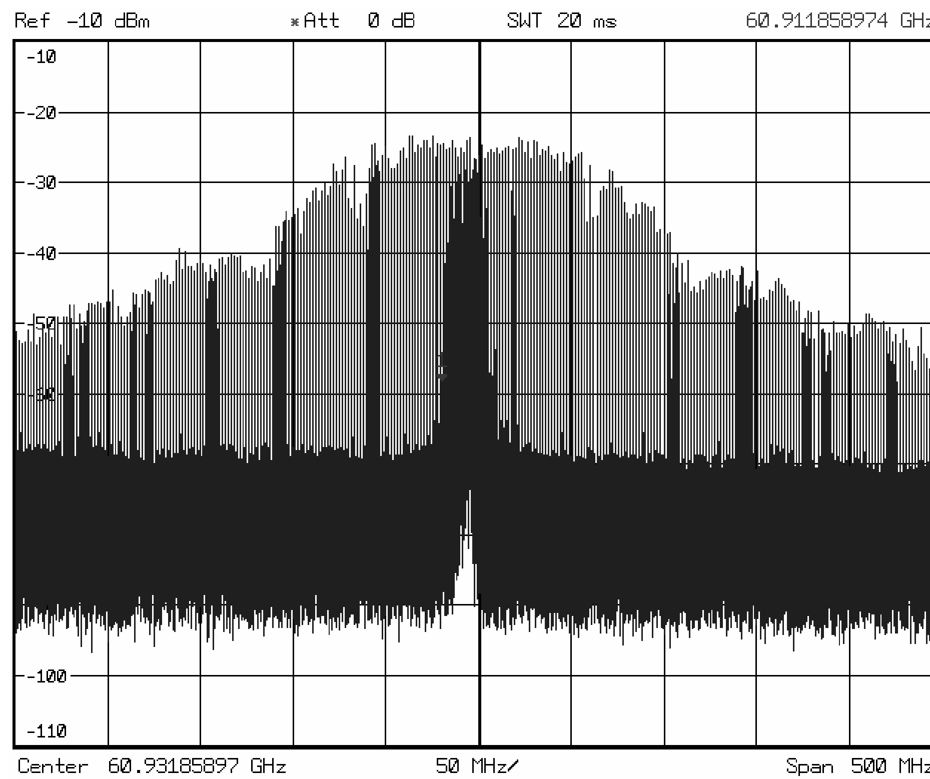
UWB transmission using 60Hz transmitter

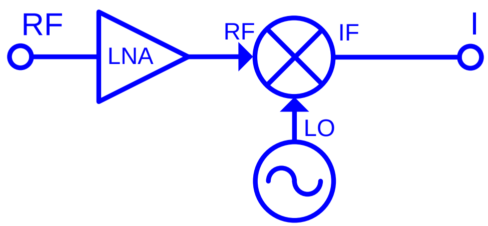


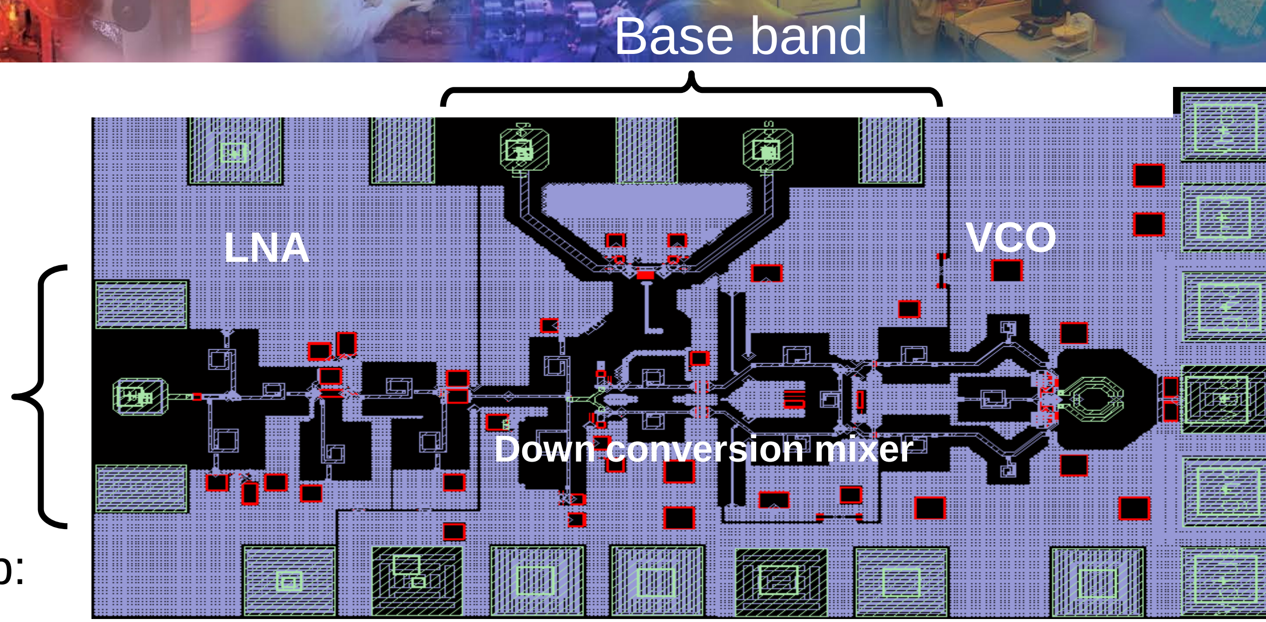


Performances of the system

- Single tone bandwidth ~ 15 GHz

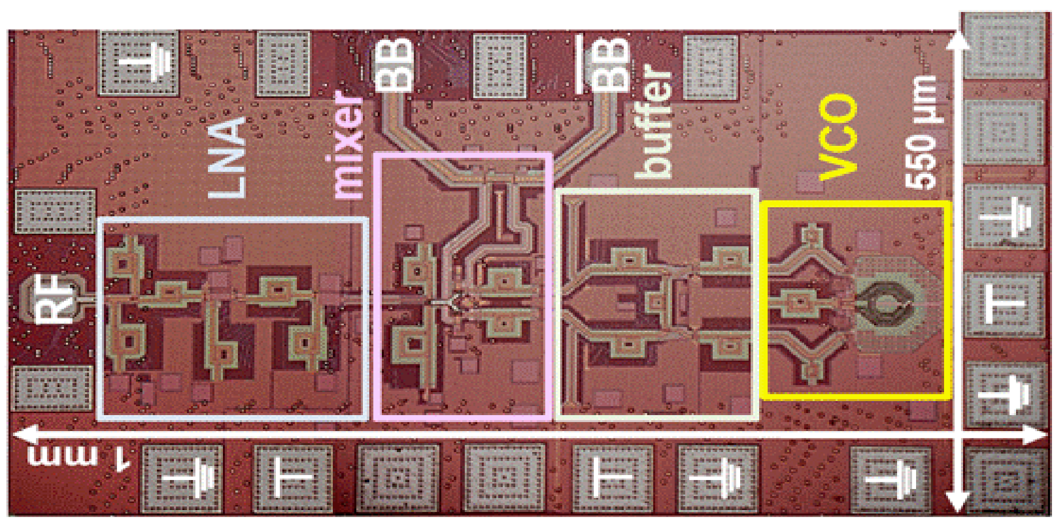
Low power 60GHz CMOS 65 nm receiver





Performances of the chip:

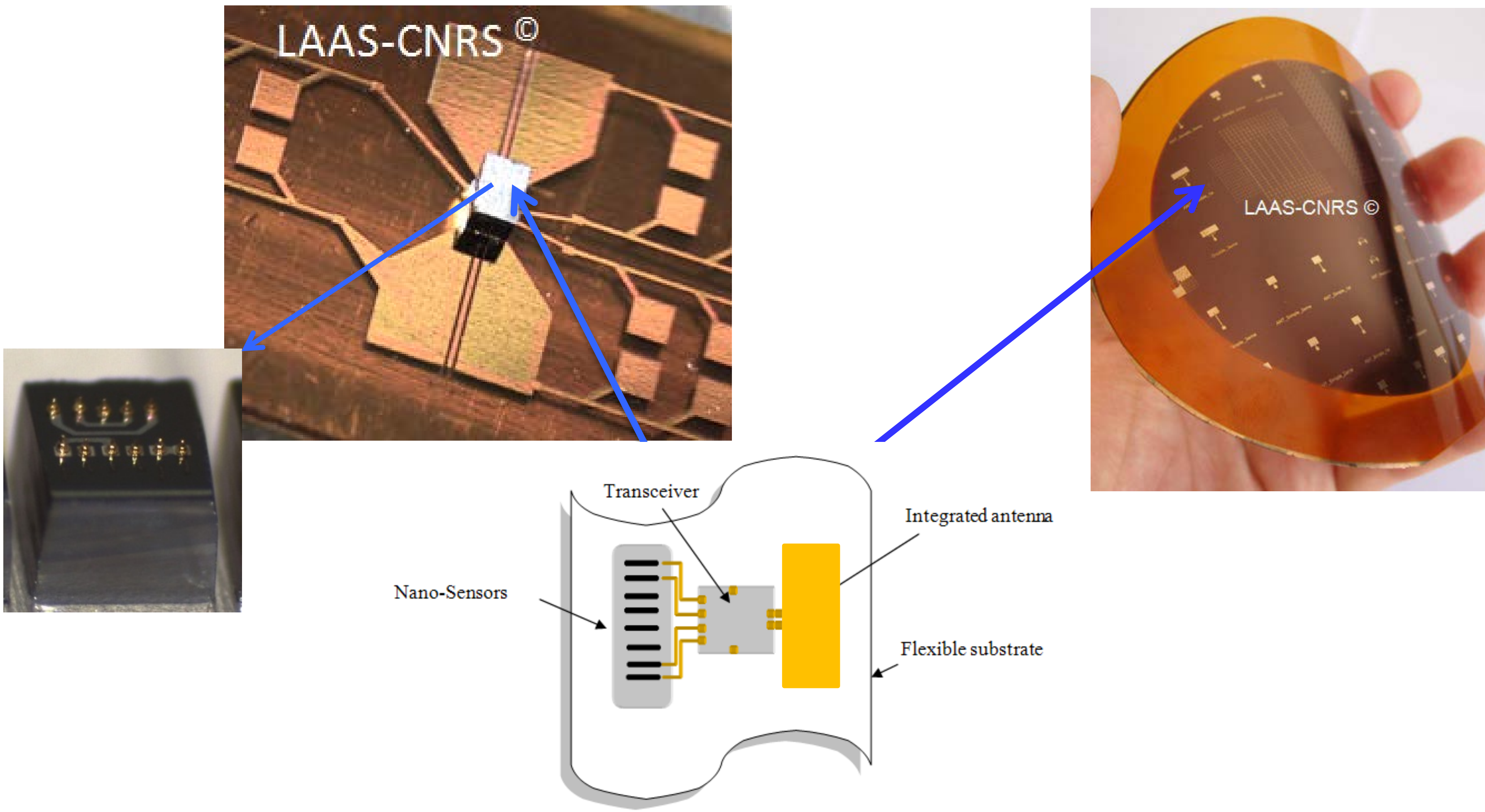
- Bias Voltage = 1.2 V
- **Power consumption = 43 mW**
- Max conversion gain ~ 30dB
- Bandwidth ~ 5 GHz
- Size: 0.55 mm^2



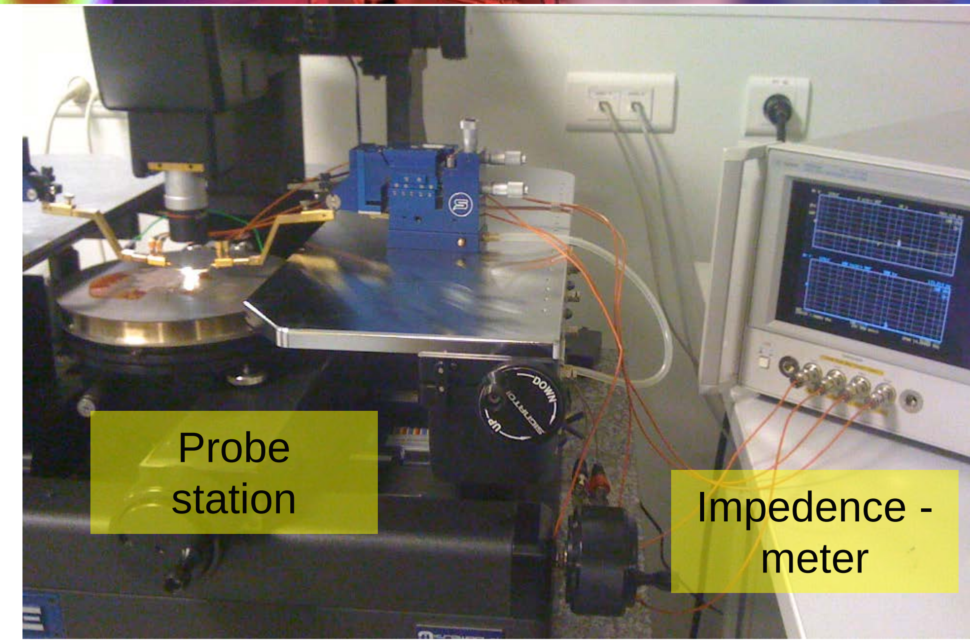
System integration for wireless sensor communicating node

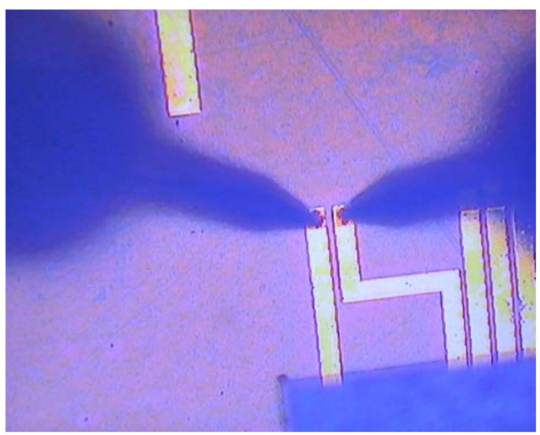
Flexible substrate integration

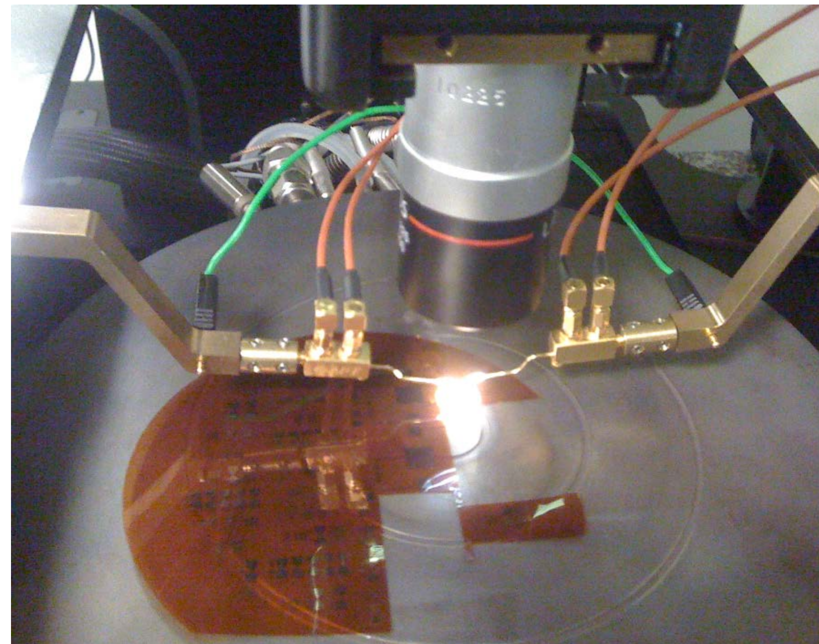
-**Technological choice:** material selection, technological process set-up
- **60GHz electrical interconnections:** Design and fabrication of test structures



Flip Chip Characterization

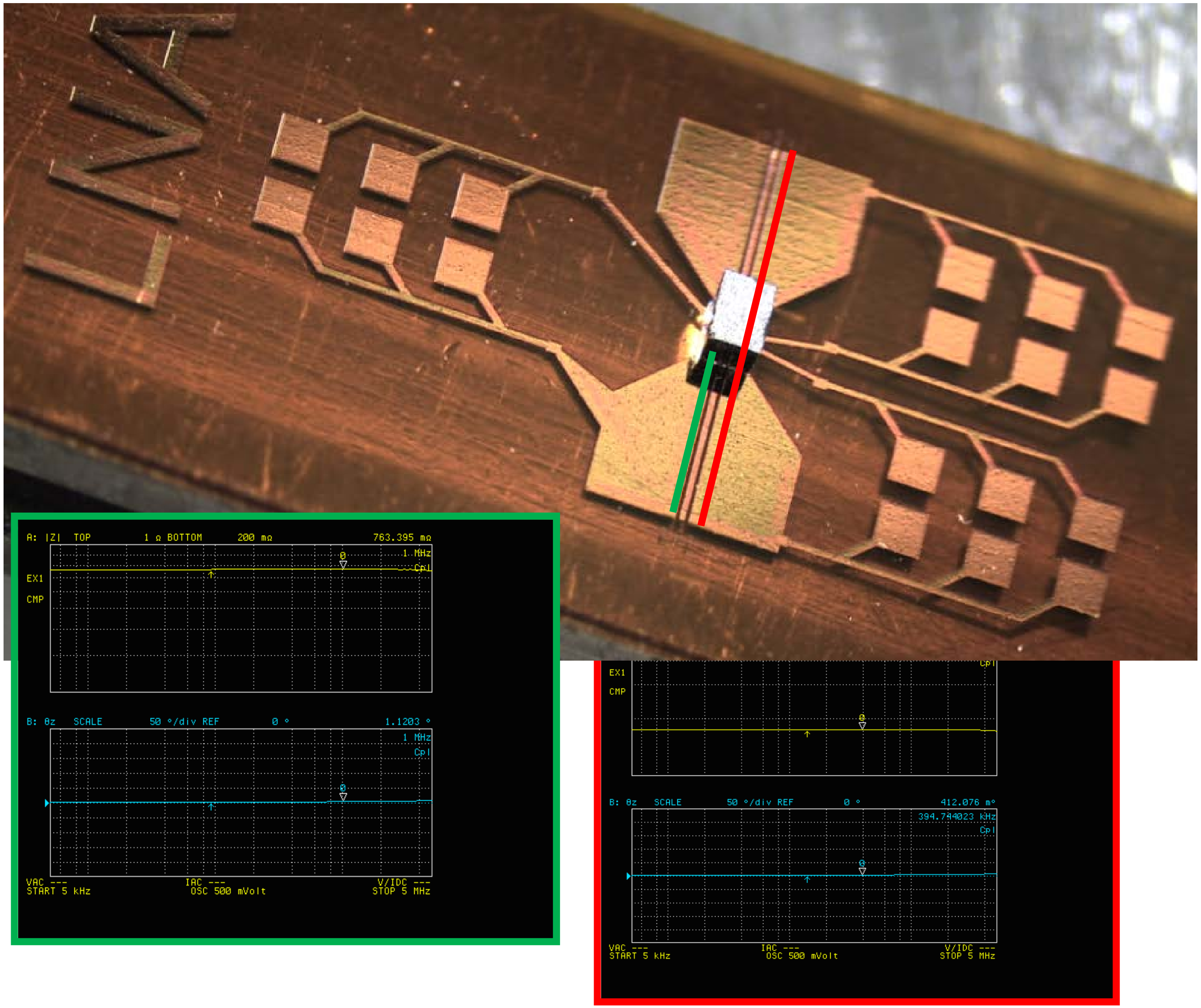


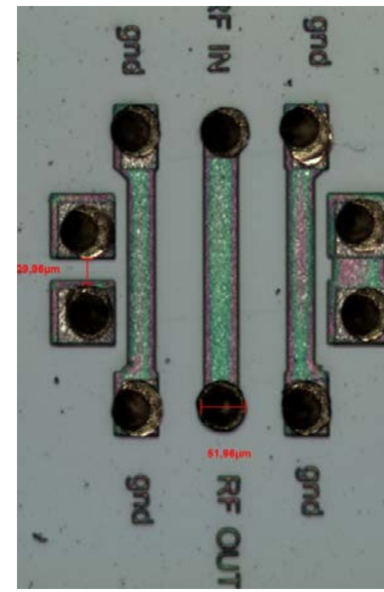




Structures under test

Flip Chip Characterization

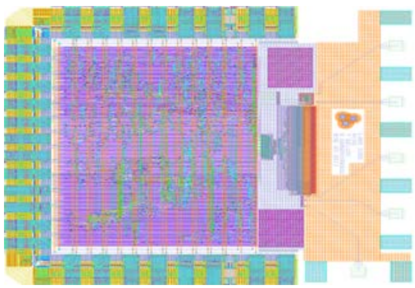




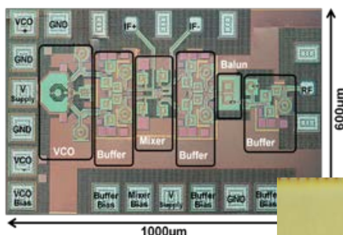
- Bump ~ 15 mΩ
- RF loses < 1 dB

Toward low power 60GHz IR UWB communication systems and flexible substrate integration

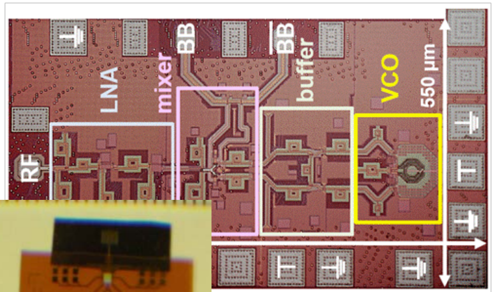
- New 3D packaging : complete communicating node integration on flexible substrate.



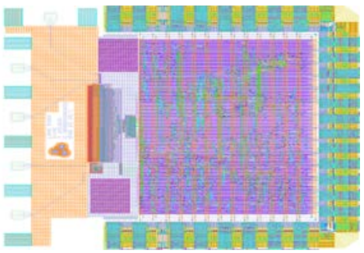
MAC layer and IR-UWB PHY layer with DAC/ADC (≈50 mW)



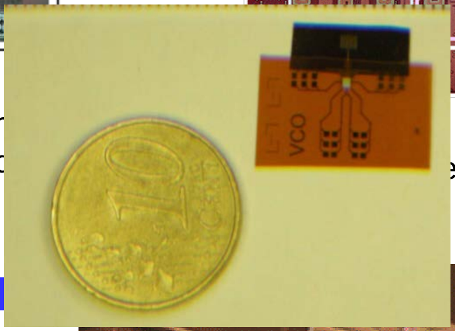
60GHz CMOS em
mW today in our c

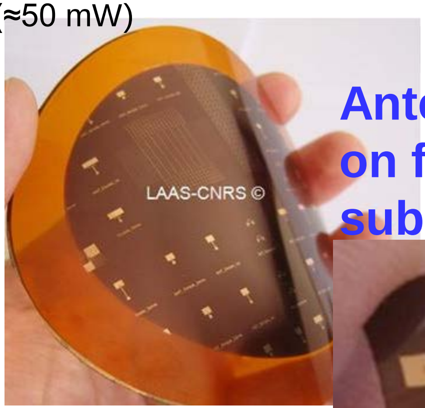


receiver (≈ 43mW
esign)

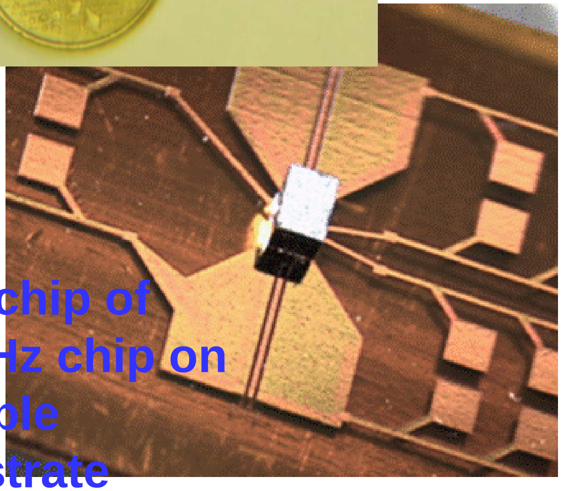


MAC layer and IR-UWB PHY layer with DAC/ADC (≈50mW)





Antenna at 60GI on flexible substrate



Flip chip of 60GHz chip on flexible substrate

Major advantage of flexible substrate integration : facility to deploy the WSN nodes for any application

Conclusion

- Wireless Sensor Network solution proposed :
  - IR-UWB reconfigurable emitter and receiver developed on FPGA
  - Impulse radio UWB transceiver on ASIC developed → very low power
  - Cross-layering MAC –PHY
  - Clock Synchronization
  - 60GHz architectures developed on ASIC in CMOS 65nm technology
  - SoC Architectures - flexible substrate integration
  - WSN simulator using UWB-impulse radio developed → determine the best network topology for one application

Thank you for your attention !